Patent Claims:

1. A semiconductor wafer, comprising a substrate wafer made of silicon and an epitaxial layer deposited thereon, characterized in that the substrate wafer has a resistivity of from 0.1 to 50 Ωcm, an oxygen concentration of less than $7.5*10^{17}$ $atcm^{-3}$ and a nitrogen concentration of from $1*10^{13}$ to $5*10^{15}$ $atcm^{-3}$, and the epitaxial layer has a thickness of from 0.2 to 1.0 µm and has a surface on which fewer than 30 LLS defects with a size of more than 0.085 µm can be detected.

2. The semiconductor wafer as claimed in claim 1, characterized in that the oxygen concentration of the substrate wafer is less than $6.5*10^{17}$ $atcm^{-3}$.

3. The semiconductor wafer as claimed in claim 1 or claim 2, characterized in that the nitrogen concentration of the substrate wafer lies in a range of from $1*10^{14}$ to $5*10^{14}$ $atcm^{-3}$.

4. A process for producing a semiconductor wafer with an epitaxial layer by depositing the layer on a substrate wafer made of silicon, characterized by a sequence of steps comprising:
the provision of the substrate wafer, the substrate wafer having a resistivity of from 0.1 to 50 Ωcm, an oxygen concentration of less than $7.5*10^{17}$ $atcm^{-3}$ and a nitrogen concentration of from $1*10^{13}$ to $5*10^{15}$ $atcm^{-3}$;
the heating of the substrate wafer in a deposition reactor to a deposition temperature of at least 1120°C; and
immediately after the deposition temperature has been reached, the deposition of the epitaxial layer with a thickness of from 0.2 to 1.0 µm.

5. The process as claimed in claim 4, characterized in that a single crystal is pulled from a melt in accordance with the Czochralski process, and at least 90 min elapse before the single crystal has passed through the temperature range from 1050 to

900°C, the single crystal serving as a source for the provision of the substrate wafer, and the deposition temperature during the deposition of the epitaxial layer is from 1120 to 1170°C.

6. The process as claimed in claim 5, characterized in that the deposition temperature is from 1130 to 1160°C.

7. The process as claimed in claim 4, characterized in that a single crystal is pulled from a melt in accordance with the Czochralski process and not more than 40 min elapse before the single crystal, with application of forced cooling, has passed through the temperature range from 1050 to 900°C, the single crystal serving as a source for the provision of the substrate wafer, and the deposition temperature during the deposition of the epitaxial layer is from 1120 to 1200°C.

8. The process as claimed in claim 7, characterized in that the deposition temperature is from 1130 to 1190°C.

9. The process as claimed in one of claims 4 to 8, characterized in that the substrate wafer is heated to the deposition temperature in a gas atmosphere, the gas atmosphere being selected from a group of gases which includes hydrogen, argon, helium and any desired mixtures of the gases mentioned.

10. The process as claimed in one of claims 4 to 9, characterized in that the epitaxial layer is deposited in a deposition atmosphere containing a deposition gas and a dopant gas, the deposition gas being selected from a group of gases which includes trichlorosilane, silane, dichlorosilane, tetrachlorosilane and any desired mixtures of the gases mentioned, and the dopant gas being selected from a group of gases which includes diborane, phosphine and arsine.

11. The process as claimed in one of claims 4 to 10, characterized in that the epitaxial layer is deposited within a deposition time of from 1 to 10 s.

12. The process as claimed in one of claims 4 to 11, characterized in that the deposition reactor is subjected to cleaning with an etching gas or plasma at the earliest after an epitaxial layer has been deposited on 50 substrate wafers in succession.